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Dag Johansen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application for:

Steven Teig, et al.

Serial No.: <not assigned yet>

Filing Date: <not assigned yet>

For: METHOD AND ARRANGEMENT FOR LAYOUT AND MANUFACTURE OF GRIDLESS NON MANHATTAN SEMICONDUCTOR INTEGRATED CIRCUITS

Examiner: <not assigned yet>

Group Art Unit: <not assigned yet>

PRELIMINARY AMENDMENT

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

Please amend the above-identified patent application as follows before examining the claims. This Preliminary Amendments is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application entitled "Method And Arrangement For Layout And Manufacture Of Gridless Non Manhattan Semiconductor Integrated Circuits," filed on 6/3/01. **Applicants**

respectfully request that claims 1 to 58 be canceled (pursuant to the amendment below) before calculation of the filing fee.

IN THE SPECIFICATION

On page 1, line 1, please insert--

Cross Reference to Related Applications

This application is a continuation application of United States Patent Application entitled "Method And Arrangement For Layout And Manufacture Of Gridless Non Manhattan Semiconductor Integrated Circuits," filed on 6/3/01, and having the Serial No. 09/681,775.--

IN THE TITLE:

Please replace the original title of the patent application with the revised title --Method and Arrangement For Layout and Manufacture of NonManhattan Semiconductor Integrated Circuit Using Simulated Euclidean Wiring--

IN THE ABSTRACT:

Please add the following abstract paragraph to the end of the patent application:

The present invention introduces several methods for implementing arbitrary angle wiring layers for integrated circuit manufacture with simulated Euclidean wiring. Entire routing layers may be implemented with arbitrary angle preferred wiring using simulated Euclidean wiring. In a first embodiment, the arbitrary angle wiring layers are created by routing arbitrary angle wires created from a selected ratio alternating segments of horizontal interconnect wire segments and vertical interconnect wire segments. In another embodiment, the arbitrary angle wiring layers are created by routing arbitrary angle wires created from a selected ratio alternating segments of horizontal interconnect wire segments and diagonal interconnect wire segments.

IN THE CLAIMS:

Please amend the claims in the above-identified patent application to appear as follows:

Please cancel claims 1 to 58.

59. (**Amended**) A method of simulating Euclidean wiring in an integrated circuit layout, said method comprising:

determining a preferred wiring angle for a metal layer of said integrated circuit layout;

determining a ratio of first interconnect line length along a first direction to a second interconnect line length along a second direction that is approximately 45 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle by creating interconnect wires made up of wire segments of said first interconnect line length along said first direction and wire segments of said second interconnect line length along said second direction.

60. (**Amended**) The method of claim 59 wherein said first direction is horizontal and said second direction is substantially 45 degrees from said horizontal.

61. (**Amended**) The method of according to claim 59 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of said first interconnect line length along said first direction and said second interconnect line length along said second direction.

62. (**Amended**) A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is substantially orthogonal to said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

64. (**Amended**) The method of according to claim 62 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and an a substantially orthogonal interconnect line length along said second direction.

65. (**Amended**) An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first arbitrary diagonal preferred direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal.

66. (**Amended**) The integrated circuit layout as claimed in claim 65, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

68. (**Amended**) The integrated circuit layout as claimed in claim 66, said integrated circuit layout further comprising:

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

69. (**Amended**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal.

70. (**Amended**) The method of laying out said integrated circuit layout as claimed in claim 69, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

Please add the following claims:

72. (**Added**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is substantially orthogonal to said horizontal.

73. (**Added**) The method of laying out said integrated circuit layout as claimed in claim 72, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

74. (**Added**) The method of laying out said integrated circuit layout as claimed in claim 72, said method wherein said first diagonal preferred direction is approximately forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.

REMARKS

The Applicant respectfully requests the Examiner to enter the above amendments before examining the patent application. The Applicant respectfully requests examination at the earliest possible date.

Respectfully submitted,

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Dated: 10/3/01

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The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined.

59. (**Amended**) A method of simulating Euclidean wiring in an integrated circuit layout, said method comprising:

determining a preferred wiring angle for a metal layer of said integrated circuit layout;

determining a ratio of [an] first interconnect line length along a first direction to a second [diagonal] interconnect line length along a second direction that is approximately 45 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle by creating interconnect wires made up of wire segments of said first interconnect line length along said first direction and wire segments of said second interconnect line length along said second direction.

60. (**Amended**) The method of claim 59 wherein said first direction is horizontal and said second direction is substantially 45 degrees from said horizontal.

61. (**Amended**) The method of according to claim 59 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of said first [an] interconnect line length along said first direction and [a] said second [diagonal] interconnect line length along said second direction.

62. (**Amended**) A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is [approximately 90 degrees from] substantially orthogonal to said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

64. (**Amended**) The method of according to claim 62 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and an a substantially orthogonal [orthognal] interconnect line length along said second direction.

65. (**Amended**) An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first arbitrary diagonal preferred direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal [first subsegment].

66. (**Amended**) The integrated circuit layout as claimed in claim 65, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

68. (**Amended**) The integrated circuit layout as claimed in claim 66, said integrated circuit layout further comprising:

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

69. (**Amended**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal [first subsegment].

70. (**Amended**) The method of laying out said integrated circuit layout as claimed in claim 69, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.